Remarks

Claims 1-25 are now pending in this application. The Office Action rejected claims 1-25 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,208,770, issued to Ito ("Ito"). Claims 1, 4-12 and 14-25 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,809,207, issued to Nillesen ("Nillesen"). The Office Action additionally rejected claims 2, 3 and 13 under 35 U.S.C. §112 and objected to the use of an acronym the abstract.

Applicants respectfully traverse all of the rejections, as the cited references do not disclose or suggest the invention as recited in any of claims 1-25. Generally, neither reference suggests or motivates an IIR filter that discards at least one bit from a feedback signal. The admitted absence of these claimed features within the references is attributable to their disparate purposes. The non-IRR filter devices of the references are unconcerned with the overflow mitigated by the claimed discarding of at least one bit. Nonetheless, Applicants have made amendments to the abstract and claims in deference to the Examiner and to resolve any perceived lack of clarity. Applicants respectfully submit that no new subject matter is being added by any of the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

Claim 1, which has been rejected as being unpatentable over either Ito or Nillesen, generally recites a method for discarding at least one bit from a feedback signal used by a digital IIR filter. First with respect to Ito, the Office Action admits that Ito teaches neither an IIR filter nor discarding at least one bit from the feedback signal. However, the

Office Action asserts that a roundoff function of Ito would render the bit discarding feature of the present invention as obvious. Applicants respectfully traverse this characterization, as the roundoff circuit 11 shown in Fig. 1 of Ito does not suggest or motivate discarding at least one bit. Rather, the roundoff circuit 11 "rounds off" by adding one to the one-half least significant bit (column 1, lines 53-55). It adds to the one-half least significant bit to achieve a desired, accumulated output (column 4, lines 5-10). A shifter 8 of Ito's roundoff circuit 11 ensures that the least significant bit is preserved and has a value of one (column 4, lines 5-10). Adding to a signal cannot be said to motivate or suggest discarding at least one bit of a signal as recited in claim 1. Thus, Ito actually teaches away from discarding a bit. Consequently, Ito has no need for, and does not suggest or motivate discarding of at least one bit from a feedback signal.

Moreover, Applicants traverse the assertion of the Office Action that the multiplication and accumulation functions described in Ito are suggestive of or motivate an IIR filter. IIR filters theoretically output an infinite number of non-zero values. This performance characteristic contrasts an IIR filter from other filters, whose output eventually tapers to zero. This property is enabled by virtue of a recursion coefficient present in the filter that feeds back previous outputs to calculate a current output sample. Despite their relative efficiency, conventional IIR filters are prone to overflow conditions. The IIR filter recited in claim 1 avoids overflow by discarding at least one bit from a feedback signal. The accumulator of Ito is concerned only with accumulating values and does not suggest or motivate filtering operations to theoretically output an infinite number of non-zero values.

The accumulation circuit of Ito is consequently unconcerned with IIR filter overflow considerations, let alone suggestive of them (column 1, lines 14-18). Claim 1 is therefore unobvious and patentable over Ito.

Nillesen similarly teaches neither an IIR filter nor discarding at least one bit from a feedback signal, as admitted on page 4 of the Office Action. Nillesen fails to teach such claimed features because instead of discarding a bit, it is rather directed to adding a bit to compensate for a truncation circuit 37. The truncation circuit 37 forms a necessary part of a video signal filter, but truncation by the circuit 37 results in "annoying phenomenon" (column 1, lines 22-29). Though not used in an IRR filter as claimed, a truncation circuit is required in video signal filters. Nillesen compensates by adding one to the least significant bit of a feedback signal (column 1, lines 41-47). By such addition, Nillesen actually teaches away from discarding at least one bit. There is therefore no suggestion or motivation within Nillesen of a discarding at least one bit from a feedback signal used by a digital IIR filter. Consequently, Applicants request reconsideration and allowance of claim 1, as well as of claims 2-11 that depend therefrom.

Now turning now to independent claims 12 and 23, which were rejected as being obvious over either Ito or Nillesen, both claims generally recite an apparatus configured to discard at least one bit from a feedback signal. The augmentation of the feedback signal mitigates the occurrence of overflow within a claimed digital IIR filter. For reasons similar to those discussed above regarding claim 1, neither Ito nor Nillesen motivates or suggests such features. Namely, Ito suggests and motivates only an

accumulator circuit that adds a value to and relies upon the presence of a least significant bit. Nillesen only suggests and motivates adding a value to a signal to avoid residual signal values otherwise caused by a standard truncation component of a video signal filter. Consequently, claims 12 and 23 are non-obvious for substantially the same reasons as stated above.

The remaining dependent claims include additional features that further distinguish themselves from the cited prior art. For instance, claims 13 and 15, like claims 2 and 3, generally recite storing the feedback signal with increased precision. This increased precision decreases the likelihood that the feedback signal will corrupt the output of the filter and leads to greater accuracy. Neither reference suggests or motivates storing an output with greater precision. Consequently, independent claims 12 and 23 are patentable, and their reconsideration and allowance, along with 13-22, 24 and 25 that depend therefrom are respectfully requested.

Applicants therefore submit that all pending claims are patentable over the prior art of record, and reconsideration and allowance of all pending claims are accordingly requested. If the examiner has any questions regarding the foregoing, or which might otherwise further this case on to allowance, the examiner may contact the undersigned at

(513) 241-2324. Moreover, if there are any charges or credits that are necessary to complete this communication, please apply them to deposit account 23-3000.

Respectfully submitted,

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